

PRELIMINARY

CY62167G/CY62167GE MoBL[®]

16-Mbit (1 M words × 16 bit / 2 M words × 8 bit) Static RAM with Error-Correcting Code (ECC)

Features

- Ultra-low standby current
 Typical standby current: 4.6 μA
 Maximum standby current: 16 μA
- High speed: 45 ns / 55 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- 48-pin TSOP I package configurable as 1 M × 16 or 2 M × 8 SRAM
- Available in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

Functional Description

CY62167G and CY62167GE are high-performance CMOS, low-power (MoBL[®]) SRAM devices with embedded ECC^[1]. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY62167GE device includes an ERR pin that signals a single-bit error-detection and correction event during a read cycle.

To access <u>devices</u> with a single chip enable input, assert the chip enable (CE) input LOW. To access dual chip enable devices, assert both chip enable inputs – \overline{CE}_1 as LOW and CE_2 as HIGH.

To perform data writes, assert the Write Enable ($\overline{\text{WE}}$) input LOW, and provide the data and address on the device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{19}) respectively. The Byte High Enable (BHE) and Byte Low Enable (BLE) inputs control byte writes and write data on the corresponding I/O lines to the memory location specified. BHE controls I/O₈ through I/O₁₅ and BLE controls I/O₀ through I/O₇.

To perform data reads, assert the Output Enable ($\overline{\text{OE}}$) input and provide the required address on the address lines. You can access read data on the I/O lines (I/O₀ through I/O₁₅). To <u>perform byte</u> accesses, assert the required byte enable signal (BHE or BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O₀ through I/O₁₅) are <u>placed</u> in a high-impedance state when the device is deselected (CE HIGH for a single chip enable device and \overline{CE}_1 HIGH / CE_2 LOW for a <u>dual chip enable</u> device), or the control signals are de-asserted (OE, BLE, BHE).

These devices have a unique Byte Power-down feature where, if both the Byte Enables (BHE and BLE) are disabled, the devices seamlessly switch to the standby mode irrespective of the state of the chip enables, thereby saving power.

On the CY62167GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High). See the Truth Table -CY62167G/CY62167GE on page 17 for a complete description of read and write modes.

The CY62167G and CY62167GE devices are available in a Pb-free 48-pin TSOP I package and 48-ball VFBGA packages. The logic block diagrams are on page 2.

The device in the 48-pin TSOP I package can also be configured to function as a 2 M words ×8 bit device. Refer to the Pin Configurations section for details.

Note

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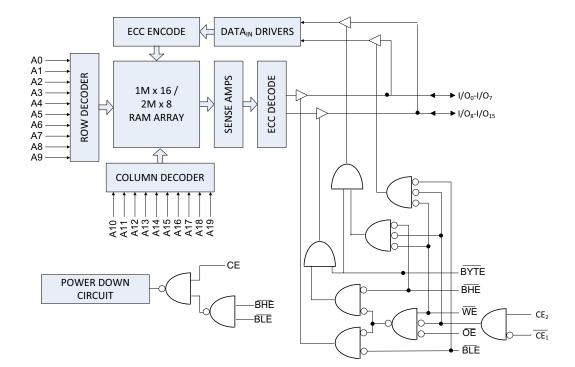
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San Jose, CA 95134-1709 • 408-943-2600 Revised September 18, 2014

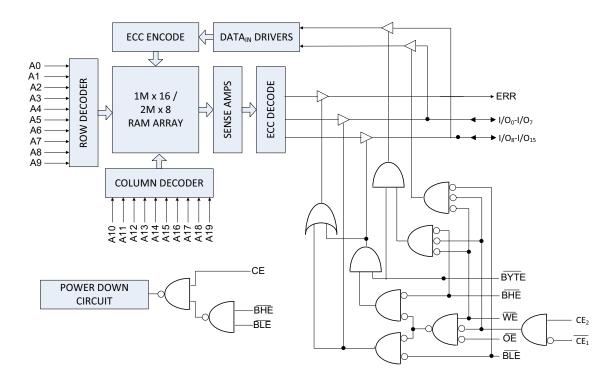
^{1.} This device does not support automatic write-back on error detection.



Logic Block Diagram – CY62167G



Logic Block Diagram – CY62167GE





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Pin Configuration – CY62167G

Figure 1. 48-ball VFBGA pinout (Dual Chip Enable without ERR) – CY62167G^[2]

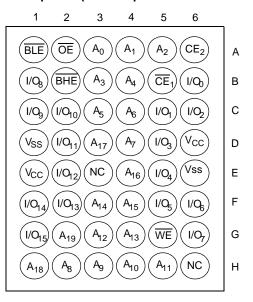


Figure 2. 48-pin TSOP I pinout (Dual Chip Enable without ERR) – CY62167G^[2, 3]

O 48 $A16$ A14 2 47 $BYTE$ A13 3 46 Vss A12 4 45 $U/O15/A20$ A11 5 44 $U/O15/A20$ A11 5 44 $U/O15/A20$ A11 6 43 $U/O14/A20$ A9 7 42 $U/O6$ A8 8 41 $U/O14$ A9 7 42 $U/O6$ A8 8 41 $U/O13$ A19 9 40 $U/O5$ NC 10 39 $U/O12$ WE 11 38 $U/O4$ CE ₂ 12 37 Vcc NC 13 36 $U/O1$ BLE 14 35 $U/O1$ A18 16 33 $U/O2$ A17 18 31 $U/O1$ A6 19 30 $U/O8$ A5 20 29 $U/O0$ A4 <t< th=""><th></th><th></th></t<>		
A14 2 47 BTE A13 3 46 Vss A12 4 45 $UO15/A20$ A11 5 44 $UO7$ A11 5 44 $UO7$ A11 6 43 $UO14/A$ A9 7 42 $UO6$ A8 8 41 $I/O13$ A19 9 40 $VO5$ NC 10 39 $UO12$ WE 11 38 $I/O4$ CE2 12 37 Vcc NC 13 36 $I/O1$ BLE 15 34 $I/O10$ A18 16 33 $I/O2$ A17 17 32 $I/O9$ A7 18 31 $I/O1$ A6 19 30 $I/O8$ A5 20 29 $I/O0$	0	10
A11 5 44 $1/07$ A10 6 43 $1/07$ A9 7 42 $1/06$ A8 8 41 $1/07$ A19 9 40 $1/05$ NC 10 39 $1/05$ NC 10 39 $1/07$ WE 11 38 $1/04$ CE ₂ 12 37 $1/07$ NC 13 36 $1/011$ BHE 14 35 $1/030$ A18 16 33 $1/020$ A17 17 32 $1/090$ A7 18 31 $1/011$ A6 19 30 $1/008$ A5 20 29 $1/000$		48 A16
A11 5 44 $1/07$ A10 6 43 $1/07$ A9 7 42 $1/06$ A8 8 41 $1/07$ A19 9 40 $1/05$ NC 10 39 $1/05$ NC 10 39 $1/07$ WE 11 38 $1/04$ CE ₂ 12 37 $1/07$ NC 13 36 $1/011$ BHE 14 35 $1/030$ A18 16 33 $1/020$ A17 17 32 $1/090$ A7 18 31 $1/011$ A6 19 30 $1/008$ A5 20 29 $1/000$		47 BYTE
A11 5 44 $1/07$ A10 6 43 $1/07$ A9 7 42 $1/06$ A8 8 41 $1/07$ A19 9 40 $1/05$ NC 10 39 $1/05$ NC 10 39 $1/07$ WE 11 38 $1/04$ CE ₂ 12 37 $1/07$ NC 13 36 $1/011$ BHE 14 35 $1/030$ A18 16 33 $1/020$ A17 17 32 $1/090$ A7 18 31 $1/011$ A6 19 30 $1/008$ A5 20 29 $1/000$	A13 🗖 3	46 – Vss
A10 6 43 μ 1014 A9 7 42 μ 106 A8 8 41 μ 1013 A19 9 40 μ 105 NC 10 39 μ 1012 WE 11 38 μ 104 CE2 12 37 ν 0c NC 13 36 μ 011 BHE 14 35 μ 003 BLE 15 34 μ 0010 A18 16 332 μ 029 A17 17 32 μ 009 A7 18 31 101 A6 19 30 μ 008 A5 20 29 μ 00	A12 🗖 4	45 I /O15/A20
A9 7 $42 \ge 1/06$ A8 8 $41 \ge 1/013$ A19 9 $40 \ge 1/013$ NC 10 39 \ge 1/012 WE 11 38 \ge 1/04 CE ₂ 12 37 \neg Vec NC 13 36 \neg 1/011 BHE 14 35 \neg 1/03 BLE 15 34 \neg 1/010 A18 16 33 \neg 1/02 A17 17 32 \neg 1/09 A7 18 31 \neg 1/01 A6 19 30 \neg 1/08 A5 20 29 \neg 1/00	A11 🗖 5	44 🗖 1/07
A8 B 41 $V013$ A19 9 40 $V05$ NC 10 39 $V012$ WE 11 38 $V04$ CE ₂ 12 37 Vcc NC 41 35 $V004$ BHE 14 35 $V001$ BHE 15 34 $V010$ A18 16 33 $V01$ A7 4 19 30 $V01$ A5 20 29 $V00$ $V00$ A5 20 29 $V00$		43 🗖 I/O14
A19 9 40 $VO5$ NC 10 39 $VO12$ WE 11 38 $VO4$ CE2 12 37 Vcc NC 13 36 $VO11$ BHE 14 35 $V03$ BLE 15 34 $V02$ A18 16 33 $V02$ A7 18 31 $V01$ A6 19 30 $V08$ A5 21 28 VOF		42 🗖 1/06
$\begin{array}{cccccccccccccccccccccccccccccccccccc$		41 🗖 I/O13
BHE II 14 35 II /03 BLE II 15 34 II /010 A18 II 16 33 II /02 A17 II 17 32 II /09 A7 II 18 30 II /01 A6 II 9 30 II /01 A5 II 20 29 II /00 A4 II 21 28 II /0F	A19 🗖 9	40 🗖 1/05
BHE II 14 35 II /03 BLE II 15 34 II /010 A18 II 16 33 II /02 A17 II 17 32 II /09 A7 II 18 30 II /01 A6 II 9 30 II /01 A5 II 20 29 II /00 A4 II 21 28 II /0F	<u>NC</u> = 10	39 🗖 I/O12
BHE II 14 35 II /03 BLE II 15 34 II /010 A18 II 16 33 II /02 A17 II 17 32 II /09 A7 II 18 30 II /01 A6 II 9 30 II /01 A5 II 20 29 II /00 A4 II 21 28 II /0F	WE 🗖 11	38 🗖 1/04
BHE II 14 35 II /03 BLE II 15 34 II /010 A18 II 16 33 II /02 A17 II 17 32 II /09 A7 II 18 30 II /01 A6 II 9 30 II /01 A5 II 20 29 II /00 A4 II 21 28 II /0F	CE ₂ - 12	37 🗖 Vcc
BHE II 14 35 II /03 BLE II 15 34 II /010 A18 II 16 33 II /02 A17 II 17 32 II /09 A7 II 18 30 II /01 A6 II 9 30 II /01 A5 II 20 29 II /00 A4 II 21 28 II /0F	NC = 13	36 🗖 I/O11
A18 16 $33 = 1/02$ A17 17 $32 = 1/09$ A7 G $31 = 1/01$ A6 19 $30 = 1/08$ A5 E 20 $29 = 1/00$ A4 E 21 $28 = 1/0F$	BHE 🗖 14	35 🗖 1/03
A18 \Box 16 33 \Box $VO2$ A17 \Box 17 32 \Box $VO9$ A7 \Box 18 31 \Box $VO1$ A6 \Box 19 30 \Box $VO8$ A5 \Box 20 29 \Box $VO8$ A4 \Box 21 28 \Box OF		34 🗖 1/010
A17 $32 = 1/09$ A7 18 A6 19 30 $1/08$ A5 20 A4 21	A18 🗖 16	33 🗖 I/O2
A6 \Box 19 30 \Box $V08$ A5 \Box 20 29 $U00$ A4 \Box 21 28 \Box	A17 🗖 17	32 🗖 1/09
A6 \Box 19 30 \Box $V08$ A5 \Box 20 29 $U00$ A4 \Box 21 28 \Box	A7 🗖 18	31 🗖 1/01
A5 H 20 29 H <u>1/00</u> A4 H 21 28 H 0F	A6 🗖 19	30 🗖 1/08
	A5 🖿 20	29 = I/O0
A3 \square 22 $27 \vdash Vss$ A2 \square 23 $26 \vdash CE_1$ A1 $= 24$ $25 \vdash A0$	A4 🗖 21	28 🗖 OF
A2 \overrightarrow{a} 23 26 \overrightarrow{c}	A3 🖿 22	27 🗖 Vss
A1 – 24 25 – A0		26 – CE
		25 – A0

- NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
- Tie the BYTE pin in the 48-pin TSOP I package to V_{CC} to use the device as a 1 M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2 M ×8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M ×8 configuration, pin 45 is the extra address line A20, while BHE, BLE, and I/O₈ to I/O₁₄ pins are not used and can be left floating.



Pin Configuration – CY62167GE

Figure 3. 48-ball VFBGA pinout (Single Chip Enable with ERR) – CY62167GE^[4]

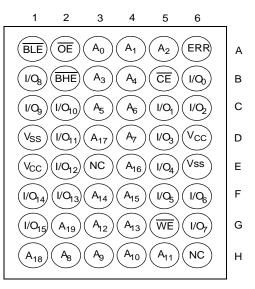
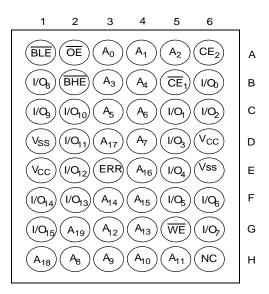


Figure 4. 48-ball VFBGA pinout (Dual Chip Enable with ERR) – CY62167GE^[4]



Note

4. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.



Pin Configuration – CY62167GE (continued)

Figure 5. 48-pin TSOP I pinout (Dual Chip Enable with ERR) – CY62167GE^[5, 6]

A15 1 48 A16 A14 2 47 BYTE A13 3 46 BYTE A13 3 46 Vss A12 4 45 I/O15/A20 A11 5 44 I/O7 A10 6 43 I/O14 A9 7 42 I/O6 A8 8 41 I/O13 A19 9 40 I/O5 NC 10 39 I/O13 A19 9 40 I/O5 WE 11 03 I/O13 A19 9 40 I/O5 WE 11 38 I/O4 CE 12 37 Vcc ERRE 13 36 I/O1 BHE 14 35 I/O3 BHE 15 34 I/O1 A6 19 30 I/O2 A7 18 01 100 A4 20 29 I/O0	0	
A14 2 47 BYTE A13 3 46 Vss A12 4 45 I/015/A20 A11 5 44 I/07 A10 6 43 I/014/ A9 7 42 I/06 A8 8 41 I/013 A19 9 40 I/05 NC 10 39 I/012 WE 11 I/013 39 I/04 C2 12 37 Vcc ERRE 13 36 I/011 BHE 14 I/010 34 I/010 A18 16 31 I/02 I/02 A7 17 32 I/09 I/01 A6 19 30 I/01 I/03 A5 20 29 I/000 24 OE A3 22 02 29 I/00	A15 1	48 416
A12 4 45 I/O15/A20 A11 5 44 I/O7 A10 6 43 I/O14 A9 7 42 I/O6 A8 8 41 I/O13 A19 9 40 I/O12 WE 10 39 I/O12 WE 11 38 I/O4 CE2 12 37 Vcc ERR 13 36 I/O11 BHE 14 35 I/O13 BHE 16 33 I/O1 A17 17 32 I/O9 A7 18 31 I/O1 A6 19 30 I/O1 A5 20 29 I/O0 A4 21 28 OE A3 22 27 Vss		
A12 4 45 I/O15/A20 A11 5 44 I/O7 A10 6 43 I/O14 A9 7 42 I/O6 A8 8 41 I/O13 A19 9 40 I/O12 WE 10 39 I/O12 WE 11 38 I/O4 CE2 12 37 Vcc ERR 13 36 I/O11 BHE 14 35 I/O13 BHE 16 33 I/O1 A17 17 32 I/O9 A7 18 31 I/O1 A6 19 30 I/O1 A5 20 29 I/O0 A4 21 28 OE A3 22 27 Vss		
A11 5 44 μ I/O7 A10 6 43 μ I/O14 A9 7 42 μ I/O13 A19 9 40 μ I/O5 NC 100 39 μ I/O13 A19 9 40 μ I/O5 NC 100 39 μ I/O12 WE 11 38 μ I/O4 CE2 12 37 Vcc ERRE 13 36 μ I/O1 BHE 14 35 μ I/O1 A18 16 33 μ I/O1 A71 17 32 μ I/O9 A7 18 31 μ I/O1 A6 19 30 20 29 μ I/O0 A4 21 22 27 Vgs		
A10 6 43 $=$ 10014 A9 7 42 $=$ 1006 A8 8 41 $=$ 1003 A19 9 40 $=$ 1003 NC 10 39 $=$ 1012 WE 11 38 $=$ 104 CE2 12 37 $=$ Vcc ERR 13 $=$ 1001 38 $=$ 1001 BLE 14 35 $=$ 1003 BLE 15 34 $=$ 1001 A18 16 33 $=$ 1002 A17 17 32 $=$ 1009 A7 18 31 $=$ 101 A5 20 29 $=$ 1000 A4 21 28 0E A3 22 27 $=$ Vss		43 I /015/A20
A9 T 42 I/O6 A8 41 I/O13 A19 9 40 I/O5 NC 10 39 I/O12 WE 11 38 I/O4 CE_p 12 37 V/cc ERR 13 36 I/O11 BIE 14 35 I/O13 BLE 15 34 I/O10 A17 17 32 I/O9 A7 18 31 I/O1 A6 19 30 I/O8 A5 20 29 I/O0 A4 21 28 OE A3 22 27 Vss		44 = 1/07
A8 = 8 41 = I/013 A19 9 40 = I/05 NC = 10 39 = I/012 WE = 11 38 = I/04 CE2 12 37 = Vcc ERRE 13 36 = I/011 BHE 14 35 = I/033 BLE 15 34 = I/010 A18 16 33 = I/029 A7 17 32 = I/09 A7 18 31 = I/01 A6 19 30 = I/08 A5 A3 22 22 29 = I/00 A4 21 28 OE A3 =		43 = 1/014
A19 9 40 $VO5$ NC 10 39 $VO5$ WE 11 38 $VO4$ CE2 12 37 Vcc ERR 13 36 $VO11$ BHE 14 35 $IO3$ BLE 15 34 $IO02$ A18 16 33 $IO2$ A17 17 32 $IO9$ A7 18 31 $IO1$ A6 19 30 $IO8$ A5 20 29 $IO0$ A4 21 28 OE A3 22 27 Vss		42 = 1/06
NC $= 10$ 39 $= 1/012$ WE $= 11$ 38 $= 1/04$ CE2 $= 12$ 37 $= 1/03$ BHE 13 36 $= 1/011$ BHE 14 35 $= 1/03$ BLE 15 34 $= 1/012$ A18 16 33 $= 1/02$ A7 $= 18$ 31 $= 1/01$ A6 $= 19$ 30 $= 1/08$ A5 $= 20$ 29 $= 1/00$ A4 $= 2/1$ $= 28$ $= OE$ A3 $= 22$ $= 27$ $= 75$		
WE 11 38 $V/04$ CE2 12 37 V/cc ERRE 13 36 $V/01$ BHE 14 35 $V/03$ BLE 15 34 $V/010$ A18 16 32 $V/09$ A7 17 32 $V/09$ A7 18 31 $V/01$ A6 19 30 $V/08$ A5 20 29 $V/00$ A4 21 28 OE A3 22 27 $V ss$	A19 = 9	40 🗖 1/05
BHE = 14 35 = 1/03 BLE = 15 34 = 1/010 A18 = 16 33 = 1/02 A17 = 17 32 = 1/09 A7 = 18 31 = 1/01 A6 = 19 30 = 1/08 A5 = 20 29 = 1/00 A4 = 21 28 = OE A3 = 22 27 = Vss	$\underline{NC} = 10$	39 = 1/O12
BHE = 14 35 = 1/03 BLE = 15 34 = 1/010 A18 = 16 33 = 1/02 A17 = 17 32 = 1/09 A7 = 18 31 = 1/01 A6 = 19 30 = 1/08 A5 = 20 29 = 1/00 A4 = 21 28 = OE A3 = 22 27 = Vss	WE 🗖 11	38 🗖 I/O4
BHE = 14 35 = 1/03 BLE = 15 34 = 1/010 A18 = 16 33 = 1/02 A17 = 17 32 = 1/09 A7 = 18 31 = 1/01 A6 = 19 30 = 1/08 A5 = 20 29 = 1/00 A4 = 21 28 = OE A3 = 22 27 = Vss	CE ₂ 🗖 12	37 🗖 Vcc
BLE 15 34 P VO10 A18 16 33 I/O2 A17 17 32 P VO9 A7 18 31 I VO1 A6 19 30 I VO8 A5 20 29 I O0 A4 21 28 OE A3 22 VSs	ERR = 13	36 🗖 I/O11
BLE 15 34 I/O10 A18 16 33 I/O2 A17 17 32 I/O9 A7 18 31 I/O1 A6 19 30 I/O8 A5 20 29 I/O0 A4 21 28 OE A3 22 27 Vss	BHE 🗖 14	35 🗖 I/O3
A18 16 $33 \Rightarrow 1/02$ A17 17 $32 \Rightarrow 1/09$ A7 $= 18$ $31 \Rightarrow 1/01$ A6 $= 19$ $30 \Rightarrow 1/08$ A5 $= 20$ $29 \Rightarrow 1/00$ A4 $= 21$ $28 \Rightarrow OE$ A3 $= 22$ $= 77 \Rightarrow Vss$	BLE 🗖 15	34 🗖 I/O10
A7 $=$ 18 31 $=$ $1/01$ A6 $=$ 19 30 $=$ $1/08$ A5 $=$ 20 29 $=$ $1/00$ A4 $=$ 21 28 $=$ OE A3 $=$ 22 $=$ 27 $=$ Vss	A18 🗖 16	33 🗖 1/02
A6 $=$ 19 30 $=$ $IO8$ A5 $=$ 20 29 $=$ $IO0$ A4 $=$ 21 28 $=$ OE A3 $=$ 22 $=$ 27 $=$ Vss		32 🗖 1/09
A5 \blacksquare 20 $29 \Rightarrow 1/00$ A4 \blacksquare 21 $28 \Rightarrow OE$ A3 \blacksquare 22 $27 \Rightarrow Vss$		31 🗖 1/01
A5 \blacksquare 20 $29 \Rightarrow 1/00$ A4 \blacksquare 21 $28 \Rightarrow OE$ A3 \blacksquare 22 $27 \Rightarrow Vss$		30 🗖 1/08
A4 c 21 28 c 0E A3 c 22 27 b Vss	A5 🗖 20	29 🗖 1/00
A3 d 22 27 b Vss	A4 🗖 21	28 🗖 OE
A2 $=$ 23 26 $=$ \overline{CE}_{4}		27 🗖 Vss
	A2 🗖 23	26 🗖 CE1
A2 $= 23$ $26 = \overline{CE_1}$ A1 $= 24$ $25 = A0$	A1 🗖 24	25 = A0

Notes 5. NC pins are not connected internally to the die and are typically used for address expansion to a higher density device. Refer to the respective datasheets for pin configuration. The USE the device as a 1 M x16 SRAM. The 48-pin TSOP I package can also be used as a 2 M x8 SRAM b

Tie the BYTE pin in the 48-pin TSOP I package to V_{CC} to use the device as a 1 M ×16 SRAM. The 48-pin TSOP I package can also be used as a 2 M ×8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M ×8 configuration, pin 45 is the extra address line A20, while the BHE, BLE, and I/O₈ to I/O₁₄ pins are not used and can be left floating. 6.



Product Portfolio

	Features and					Current Co	onsumption		
	Options	_				Operating I _{CC} , (mA)			
Product	(see the Pin	Range	V _{CC} Range (V)	Speed (ns)	f = f _{max}		_ Standby, I _{SB2} (μA)		
	Configurations section)				Typ ^[7]	Max	Typ ^[7]	Max	
CY62167G(E)18	Single or dual	Industrial	1.65 V–2.2 V	55	29	32	5.5	26	
CY62167G(E)30			2.2 V–3.6 V	45	29	36	4.6	16	
CY62167G(E)	Optional ERR pin		4.5 V–5.5 V						

Note 7. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.



CY62167G/CY62167GE MoBL®

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature65 °C to + 150 °C
Ambient temperature with power applied55 °C to + 125 °C
Supply voltage to ground potential–0.5 V to 6 V
DC voltage applied to outputs in High Z state $^{[8]}$ –0.5 V to V_{CC} + 0.5 V
DC input voltage ^[8] –0.5 V to V_{CC} + 0.5 V

Output current into outputs (LOW)	
Static discharge voltage	
(MIL-STD-883, Method 3015)	>2001 V
Latch-up current	>140 mA

Operating Range

Grade	Ambient Temperature	V_{CC} ^[9]
Industrial	−40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

Deveryoter	Dee	a vin ti a v	Test Conditions			45/55 i	ns	11
Parameter	Des	cription			Min	Typ ^[10]	Max	Unit
V _{OH}	Output HIGH	1.65 V to 2.2 V	$V_{CC} = Min, I_{OH} = -0.1 mA$		1.4	-	-	V
	voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = -0.1 mA		2.0	-	_	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = -1.0 mA		2.2	-	-	
		4.5 V to 5.5 V	$V_{CC} = Min, I_{OH} = -1.0 \text{ mA}$		2.4	_	-	
	Output LOW	1.65 V to 2.2 V	$V_{CC} = Min, I_{OL} = 0.1 mA$		—	_	0.2	V
	voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 0.1 mA		_	-	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 2.1 mA		—	_	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 2.1 mA		_	-	0.4	
V _{IH}	Input HIGH	1.65 V to 2.2 V	-		1.4	-	$V_{CC} + 0.2$	V
voltage ^[8]	2.2 V to 2.7 V	-		2.0	-	$V_{CC} + 0.3$		
	2.7 V to 3.6 V	-		2.0	-	$V_{CC} + 0.3$		
		4.5 V to 5.5 V	-		2.2	_	$V_{CC} + 0.5$	
V _{IL}	Input LOW	1.65 V to 2.2 V	-		-0.2	-	0.4	V
	voltage ^[8]	2.2 V to 2.7 V	-		-0.3	-	0.6	
		2.7 V to 3.6 V	-		-0.3	-	0.8	
		4.5 V to 5.5 V	-		-0.5	_	0.8	
I _{IX}	Input leakage of	current	$GND \leq V_{IN} \leq V_{CC}$		-1.0	-	+1.0	μA
I _{OZ}	Output leakage	e current	$GND \le V_{OUT} \le V_{CC},$ Output disabled		-1.0	-	+1.0	μA
I _{CC}	V _{CC} operating	supply current	V _{CC} = Max, I _{OUT} = 0 mA, CMOS levels	f = 22.22 MHz (45 ns)	-	29.0	36.0	mA
				f = 18.18 MHz (55 ns)	-	29.0	32.0	mA
				f = 1 MHz	-	7.0	9.0	mA

Notes

Notes
 V_{IL(min)} = -2.0 V and V_{IH(max)} = V_{CC} + 2 V for pulse durations of less than 2 ns.
 Full device AC operation assumes a 100-µs ramp time from 0 to V_{CC} (min) and 200-µs wait time after V_{CC} stabilizes to its operational value.
 Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.



DC Electrical Characteristics (continued)

Over the operating range of –40 $^\circ C$ to 85 $^\circ C$

Parameter	Description Test Conditions			45/55 ns		าร	Unit
Farameter	Description				Typ ^[10]	Max	Unit
I _{SB1} ^[11]	current – CMOS inputs;	$\overline{CE}_1 \ge V_{CC} - 0.2 \text{ V or } CE_2 \le 0.2 \text{ V}$ or (\overline{BHE} and \overline{BLE}) $\ge V_{CC} - 0.2 \text{ V}$,		_	4.6	16.0	μA
	Automatic power down current – CMOS inputs $V_{IN} \ge V_{CC} - f = f_{max}$ (add $V_{CC} = 1.65$ to 2.2 V $f = 0$ (\overline{OE} , ar			_	5.5	26.0	
I _{SB2} ^[11]	SB2 ^[11] Automatic power down current – CMOS inputs $V_{CC} = 2.2$ to 3.6 V and 4.5 to 5.5 V	$\overline{CE}_1 \ge V_{CC} - 0.2V$ or	25 °C	-	4.6	6.0 ^[12]	μA
		$CE_2 \le 0.2 V \text{ or}$	40 °C	-	5.1	8.0 ^[12]	
		$(\overline{BHE} \text{ and } \overline{BLE}) \ge V_{CC} - 0.2 \text{ V},$	70 °C	-	8.4	12.0 ^[12]	
		$ \begin{array}{l} V_{\text{IN}} \geq V_{\text{CC}} - 0.2 \text{ V or } V_{\text{IN}} \leq 0.2 \\ V, \\ f = 0, V_{\text{CC}} = V_{\text{CC}(\text{max})} \end{array} $	85 °C	-	12.0	16.0	
	Automatic power down current – CMOS inputs V_{CC} = 1.65 to 2.2 V	$\label{eq:cell} \begin{split} \overline{CE}_1 \geq V_{CC} - 0.2V \text{ or } CE_2 \leq 0.2 \\ \text{or } (\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \\ V_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \\ \text{f} = 0, \ V_{CC} = V_{CC(max)} \end{split}$	V,	_	5.5	26.0	

Notes 11. Chip enables (\overline{CE}_1 and CE_2) and \overline{BYTE} must be tied to CMOS levels to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating. 12. The I_{SB2} maximum limits at 25 °C, 40 °C, and 70 °C are guaranteed by design and not 100% tested.



Capacitance

Parameter ^[13]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = V_{CC(typ)}$	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[13]	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
- JA		Still air, soldered on a 3 \times 4.5 inch, two-layer printed circuit board	31.50	57.99	°C/W
- 30	Thermal resistance (junction to case)		15.75	13.42	°C/W

AC Test Loads and Waveforms

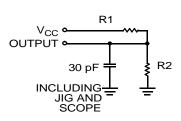
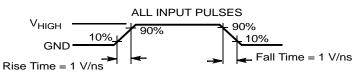


Figure 6. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R1	13500	16667	1103	1800	Ω
R2	10800	15385	1554	990	Ω
R _{TH}	6000	8000	645	639	Ω
V _{TH}	0.80	1.20	1.75	1.77	V

Note 13. Tested initially and after any design or process changes that may affect these parameters.



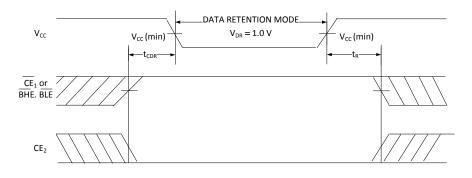
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[14]	Max	Unit
V _{DR}	V _{CC} for data retention		1.0	-	_	V
I _{CCDR} ^[15, 16]	Data retention current	$\begin{array}{l} 1.2 \ V \leq V_{CC} \leq 2.2 \ V, \\ \hline \overline{CE}_1 \geq V_{CC} - 0.2 \ V \ \text{or} \ CE_2 \leq 0.2 \ V \\ \hline \text{or} \ (\overline{BHE} \ \text{and} \ \overline{BLE}) \geq V_{CC} - 0.2 \ V, \\ \hline V_{IN} \geq V_{CC} - 0.2 \ V \ \text{or} \ V_{IN} \leq 0.2 \ V \end{array}$	_	5.5	26.0	μA
		$\begin{array}{l} 2.2 \ V < V_{CC} \leq 3.6 \ V \ or \\ 4.5 \ V \leq V_{CC} \leq 5.5 \ V, \\ \hline $	_	4.6	16.0	μA
t _{CDR} ^[17]	Chip deselect to data retention time		0	-	-	-
t _R ^[18]	Operation recovery time		45/55	—	_	ns

Data Retention Waveform

Figure 7. Data Retention Waveform ^[19]



- 14. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested. 15. Chip enables (\overline{CE}_1 and \overline{CE}_2) and BYTE must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating. 16. I_{CCDR} is guaranteed only after the device is first powered up to V_{CC}(min) and then brought down to V_{DR}.

- 17. Tested initially and after any design or process changes that may affect these parameters.
 18. Full-device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.
 19. BHE.BLE is the AND of both BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling both BHE and BLE.



Switching Characteristics

Parameter ^[20, 21]	Description	45	ns	55	Unit	
	Description	Min	Max	Min	Max	Unit
READ CYCLE						
t _{RC}	Read cycle time	45.0	-	55.0	-	ns
t _{AA}	Address to data valid / Address to ERR valid	_	45.0	_	55.0	ns
t _{OHA}	Data hold from address change / ERR hold from address change	10.0	-	10.0	-	ns
t _{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to data valid / \overline{CE} LOW to ERR valid	-	45.0	-	55.0	ns
t _{DOE}	OE LOW to data valid / OE LOW to ERR valid	_	22.0	-	25.0	ns
t _{LZOE}	OE LOW to Low-Z ^[21]	5.0	_	5.0	-	ns
t _{HZOE}	OE HIGH to High-Z ^[21, 22]	_	18.0	-	18.0	ns
t _{LZCE}	CE ₁ LOW and CE ₂ HIGH to Low-Z ^[21]	10.0	_	10.0	-	ns
t _{HZCE}	CE ₁ HIGH and CE ₂ LOW to High-Z ^[21, 22]	_	18.0	_	18.0	ns
t _{PU}	CE ₁ LOW and CE ₂ HIGH to power-up	0	_	0	-	ns
t _{PD}	CE ₁ HIGH and CE ₂ LOW to power-down	_	45.0	_	55.0	ns
t _{DBE}	BLE / BHE LOW to data valid	_	45.0	_	55.0	ns
t _{LZBE}	BLE / BHE LOW to Low-Z ^[21]	5.0	_	5.0	-	ns
t _{HZBE}	BLE / BHE HIGH to High-Z ^[21, 22]	_	18.0	_	18.0	ns
WRITE CYCLE ^{[23}	3, 24]			•	•	
t _{WC}	Write cycle time	45.0	_	55.0	-	ns
t _{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to write end	35.0	_	40.0	-	ns
t _{AW}	Address setup to write end	35.0	_	40.0	-	ns
t _{HA}	Address hold from write end	0	_	0	-	ns
t _{SA}	Address setup to write start	0	_	0	-	ns
t _{PWE}	WE pulse width	35.0	_	40.0	-	ns
t _{BW}	BLE / BHE LOW to write end	35.0	_	40.0	-	ns
t _{SD}	Data setup to write end	25.0	-	25.0	-	ns
t _{HD}	Data hold from write end	0	-	0	-	ns
t _{HZWE}	WE LOW to High-Z ^[21, 22]	_	18.0	-	20.0	ns
t _{LZWE}	WE HIGH to Low-Z ^[21]	10.0	-	10.0	-	ns

Notes

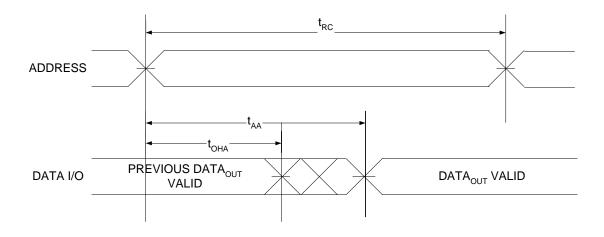
20. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \ge 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \ge 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use the output loading shown in Figure 6 on page 10, unless specified otherwise. 21. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device. 22. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state. 23. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both $= V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write. the write.

24. The minimum write cycle pulse width for WRITE Cycle 1 (WE controlled, OE LOW) should be equal to the sum of t_{HZWE} and t_{SD}

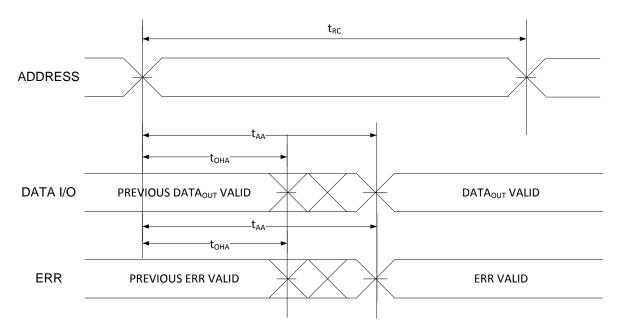


Switching Waveforms

Figure 8. Read Cycle No. 1 of CY62167G (Address Transition Controlled)^[25, 26]







Notes 25. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, \overline{BHE} or \overline{BLE} , or both = V_{IL} . 26. $\overline{\text{WE}}$ is HIGH for read cycle.



Switching Waveforms (continued)

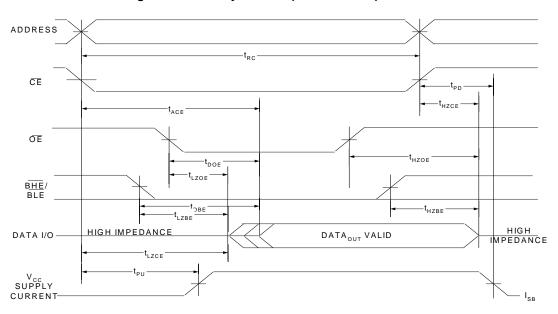
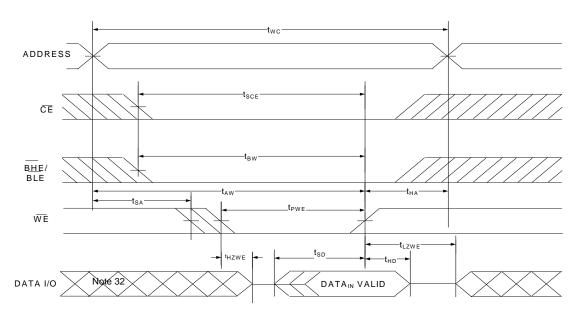


Figure 10. Read Cycle No. 2 (OE Controlled)^[27, 28, 29, 31]

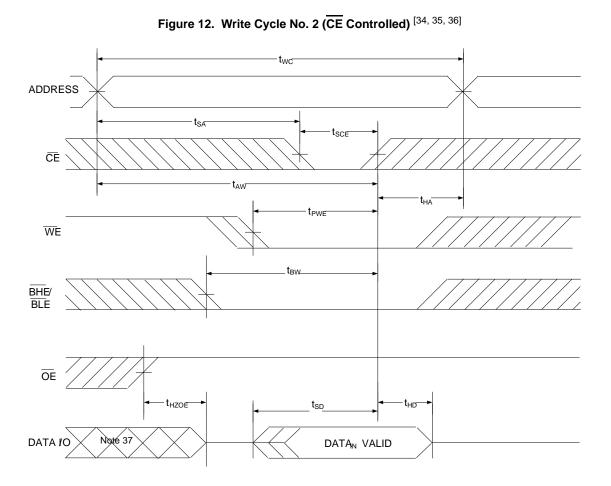




- 27. WE is HIGH for read cycle.
- 28. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 29. Address valid prior to or coincident with \overline{CE} LOW transition. 30. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} , or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 31. Data I/O is in the high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.
- 32. During this period, the I/Os are in the output state. Do not apply input signals.
- 33. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD} .



Switching Waveforms (continued)



- 34. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 35. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{EE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 36. Data I/O is in the high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.
- 37. During this period, the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

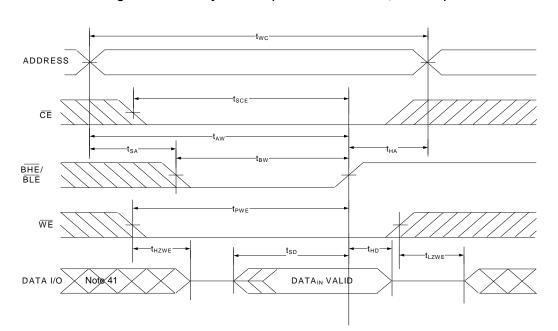
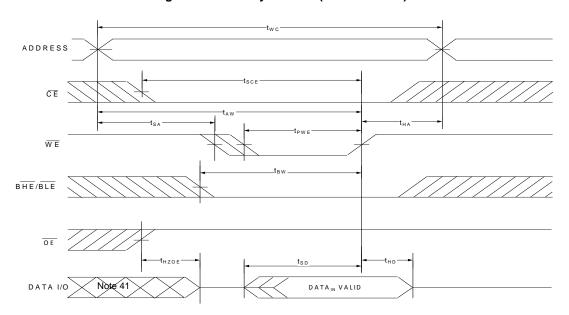


Figure 13. Write Cycle No. 4 (BHE/BLE controlled, OE LOW) ^[38, 39, 40]

Figure 14. Write Cycle No. 5 (WE controlled) ^[38, 39, 40]



- 38. Eor all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, CE is HIGH.
- 39. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 40. Data I/O is in the high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.
- 41. During this period, the I/Os are in output state. Do not apply input signals.



Truth Table - CY62167G/CY62167GE

BYTE [42]	CE ₁	CE ₂	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power	Configuration
X ^[43]	Н	X ^[43]	Х	Х	Х	Х	High-Z	Deselect/Power-down	Standby (I _{SB})	2 M × 8 / 1 M × 16
Х	X ^[43]	L	Х	Х	Х	Х	High-Z	Deselect/Power-down	Standby (I_{SB})	$2M \times 8/1M \times 16$
Х	X ^[43]	X ^[43]	Х	Х	Н	Н	High-Z	Deselect/Power-down	Standby (I _{SB})	1 M × 16
Н	L	Н	Н	L	L	L	Data Out (I/O ₀ -I/O ₁₅)	Read	Active (I _{CC})	1 M × 16
Н	L	Н	Н	L	Н	L	Data Out (I/O ₀ –I/O ₇); High-Z (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})	1 M × 16
Н	L	Н	Н	L	L	Н	High Z (I/O ₀ –I/O ₇); Data Out (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})	1 M × 16
Н	L	Н	Н	Н	L	Н	High-Z	Output disabled	Active (I _{CC})	1 M × 16
Н	L	Н	Н	Н	Н	L	High-Z	Output disabled	Active (I _{CC})	1 M × 16
Н	L	Н	Н	Н	L	L	High-Z	Output disabled	Active (I _{CC})	1 M × 16
Н	L	Н	L	Х	L	L	Data In (I/O ₀ -I/O ₁₅)	Write	Active (I _{CC})	1 M × 16
Н	L	Н	L	Х	Η	L	Data In (I/O ₀ –I/O ₇); High-Z (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})	1 M × 16
Н	L	Н	L	Х	L	Н	High-Z (I/O ₀ –I/O ₇); Data In (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})	1 M × 16
L	L	Н	Н	L	Х	Х	Data Out (I/O ₀ –I/O ₇)	Read	Active (I _{CC})	2 M × 8
L	L	Н	Н	Н	Х	Х	High-Z	Output disabled	Active (I _{CC})	2 M × 8
L	L	Н	L	Х	Х	Х	Data In (I/O ₀ –I/O ₇)	Write	Active (I _{CC})	2 M × 8

ERR Output – CY62167GE

Output	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected / outputs disabled / Write operation

Notes

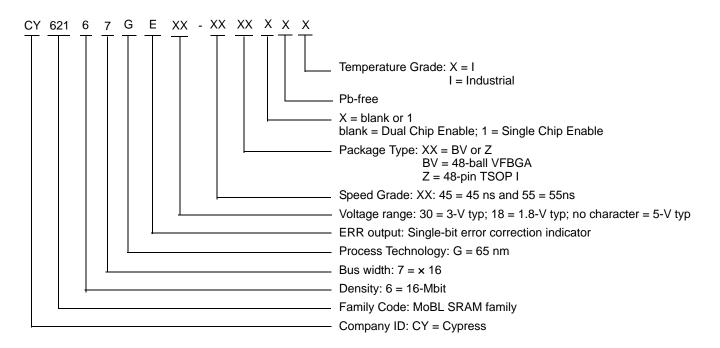
42. This pin is available only in the 48-pin <u>TSOP</u> I package. Tie the <u>BYTE</u> to V_{CC} to configure the device in the 1 M ×16 option. The 48-pin TSOP I package can also be used as a 2 M × 8 SRAM by tying the <u>BYTE</u> signal to V_{SS}.
 43. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167G30-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48, Dual Chip Enable without ERR	Industrial
	CY62167G30-45ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Package Code: Z48A, Dual Chip Enable without ERR	
	CY62167G-45ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Dual Chip Enable without ERR	
	CY62167GE30-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Dual Chip Enable with ERR output at pin E3	
	CY62167GE30-45ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Dual Chip Enable with ERR output at pin 13	
	CY62167GE-45ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Dual Chip Enable with ERR output at pin 13	
55	CY62167G18-55BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Dual Chip Enable without ERR	Industrial
	CY62167GE18-55BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Dual Chip Enable with ERR output at pin E3	

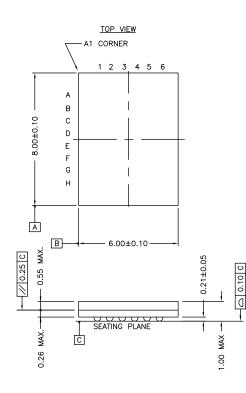
Ordering Code Definitions

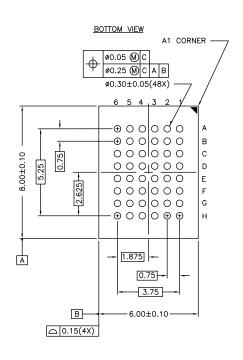




Package Diagrams

Figure 15. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150





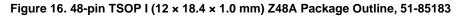
NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

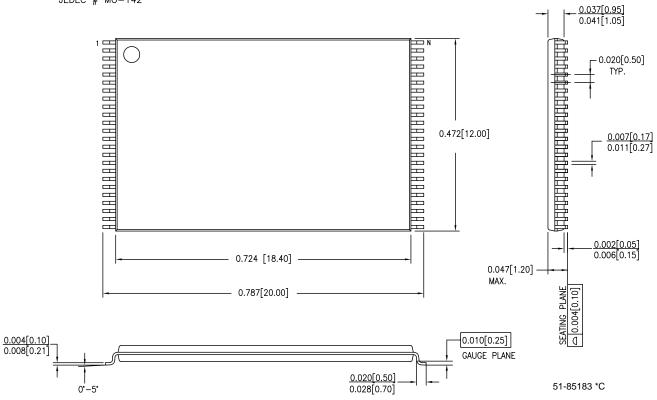


Package Diagrams (continued)



DIMENSIONS IN INCHES[MM] $\frac{\text{MIN.}}{\text{MAX.}}$

JEDEC # MO-142





Acronyms

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
OE	Output Enable
SRAM	Static random access memory
TSOP	Thin small outline package
VFBGA	Very fine-pitch ball grid array
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μS	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



Errata

This Errata is applicable for the Rev. *C silicon only.

This section describes the errata for the 16-Mbit asynchronous MoBL SRAM - CY62167G/CY62167GE - in the 65-nm process technology. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

If you have questions, contact your local Cypress Sales Representative or raise a technical support case at www.cypress.com/go/support.

Part Numbers Affected

Part Number	Device Characteristics
CY62167G (all packages and options) CY62167GE (all packages and options)	16-Mbit MoBL SRAM

CY62167G(E) Qualification Status

Product Status: Engineering Samples (**Note:** Reliability qualification is not complete. These samples are recommended to be used for engineering builds and evaluation only, and not for production builds).

CY62167G(E) SRAM Errata Summary

This table defines the errata applicability to available 16-Mbit devices.

Items	Part Numbers	Silicon Revision	Fix Status
[1] I_{SB1} , I_{SB2} and I_{CCDR} (Standby current specifications) do not meet datasheet spec	CY62167G/ CY62167GE	*C	Fixed devices available from December 14, 2014

1. I_{SB1} , I_{SB2} (Standby current) and I_{CCDR} (Data Retention Current) issue

Problem Definition

 I_{SB1} (f = fmax), I_{SB2} (f = 0) and I_{CCDR} do not meet the datasheet limits as captured in the tables below.

Parameter	Description	Test Conditions		Datasheet Typ ^[14]	Errata Typ ^[14]	Unit
[44]			1	тур	тур	
I _{SB2} ^[11]	Automatic power down	$CE_1 \ge V_{CC} - 0.2V$ or	25 °C	4.6	5.3	μA
	current – CMOS inputs V_{CC} = 2.2 to 3.6 V and 4.5 to 5.5 V	$CE_2 \le 0.2 V \text{ or}$	40 °C	5.1	5.8	
		$\begin{array}{l} (\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}, \\ V_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V}, \\ f = 0, \ V_{CC} = V_{CC(max)} \end{array}$	70 °C	8.4	9.0	
	Automatic power down current – CMOS inputs V _{CC} = 1.65 to 2.2 V	$\label{eq:cell} \begin{split} \overline{CE}_1 \geq V_{CC} &= 0.2 \text{V or } CE_2 \leq 0.2 \text{ V} \\ \text{or } (\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} &= 0.2 \text{ V}, \\ V_{\text{IN}} \geq V_{CC} &= 0.2 \text{ V or } V_{\text{IN}} \leq 0.2 \text{ V}, \\ \text{f} &= 0, \ V_{CC} &= V_{CC(\text{max})} \end{split}$		5.5	6.9	



Deremeter	Description	Tast Canditians	Datasheet	Errata	Unit
Parameter	Description	Test Conditions	Typ ^[14]	Typ ^[14]	Unit
I _{SB1} ^[11]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 to 3.6 V and 4.5 to 5.5 V	$\overline{CE}_{1} \ge V_{CC} - 0.2 \text{ V or } CE_{2} \le 0.2 \text{ V}$ or (\overline{BHE} and \overline{BLE}) $\ge V_{CC} - 0.2 \text{ V}$, $V_{IN} \ge V_{CC} - 0.2 \text{ V}$, $V_{IN} \le 0.2 \text{ V}$,	4.6	5.3	μΑ
	Automatic power down current – CMOS inputs V _{CC} = 1.65 to 2.2 V	$f = f_{max}$ (address and data only), $f = 0$ (\overline{OE} , and \overline{WE}), $V_{CC} = V_{CC(max)}$	5.5	6.9	
I _{CCDR} ^[15,16]	Data retention current	$1.2 \text{ V} \le \text{V}_{\text{CC}} \le 2.2 \text{ V},$			μΑ
		$\overline{CE}_1 \ge V_{CC} - 0.2 \text{ V or } CE_2 \le 0.2 \text{ V}$	5.5	6.9	
		or (\overline{BHE} and \overline{BLE}) $\geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$			
		2.2 V < V _{CC} \leq 3.6 V or 4.5 V \leq V _{CC} \leq 5.5 V,			
		$\overline{\text{CE}}_{1} \ge \text{V}_{\text{CC}} - 0.2 \text{ V or } \text{CE}_{2} \le 0.2 \text{ V}$	4.6	5.3	
		or (\overline{BHE} and \overline{BLE}) \geq V _{CC} – 0.2 V, V _{IN} \geq V _{CC} – 0.2 V or V _{IN} \leq 0.2 V			

Parameters Affected

Standby current specifications I_{SB1} , I_{SB2} and I_{CCDR}

Trigger Condition

When Chip Enable (s) is/are de-asserted to place the device in standby mode, the current drawn (I_{SB1} / I_{SB2}) are greater than the datasheet-specified limit.

When Chip is in data retention mode, the current drawn (I_{CCDR}) is greater than the datasheet-specified limit.

Scope of Impact

Since these are Engineering samples and are expected to be used for evaluation, a marginal increase in standby/ data retention current is not expected to have an impact. Increase in standby/ data retention currents could result in a long term effect of reduced battery life; however, since these are Engineering samples expected to be used for engineering builds and evaluation only, impact is expected to be minimal.

Workaround

Ensure adequate source of power that accounts for the increased standby current

Fix Status

Fixed devices available from December 14, 2014.



Document History Page

Rev. E	CN No.	Orig. of Change	Submission Date	Description of Change
** 3	690096	TAVA	07/26/2012	New data sheet.
	776318	AJU	10/30/2012	Updated Document title to "16-Mbit (1 M words × 16 bit / 2 M words × 8 bit Static RAM with Error-Correcting Code (ECC)". Updated Features (Included ECC feature, updated typical standby current spec). Added note #1 Corrected typos in Functional Description. Updated Logic Block Diagram – CY62167G, Logic Block Diagram – CY62167GE for better clarity. Updated Notes 2, 3, 4, 5 for better clarity. Listed all product options in Product Portfolio. Added typical values for I _{SB2} parameter. Updated Note 7 for better clarity. Updated Maximum Ratings to extend limits for 5 V device. Changed latch up current limit from 200 to 140 mA (per JEDEC limits). Updated DC Electrical Characteristics Corrected I _{OH} and I _{OL} conditions for V _{OH} and V _{OL} specifications. Added I _{CC} typical and maximum values at f = 1 MHz Changed typical spec for I _{SB1} and I _{SB2} from 2.5 μA to 3.2 μA. Split the I _{SB1} and I _{SB2} specs across multiple voltage ranges. Updated Description and Test Conditions for I _{SB1} and I _{SB2} parameters. Added Note 11 and referred it in the I _{SB1} and I _{SB2} parameters for 48 pin TSOP I package. Added values for V _{HIGH} parameters in AC Test Loads and Waveforms. Updated Data Retention Characteristics Split Test Conditions of I _{CCDR} parameter into two rows to cover multiple V _Q ranges. Changed typical spec for I _{CCDR} from 2.5 μA to 3.2 μA. Updated Data Retention Characteristics Updated Note 15 to remove byte enables. Updated Note 15 to remove byte enables. Updated Note 20, 23 for better clarity. Updated Note 20, 23 for better clarity. Updated Note 20, 23 for better clarity. Updated Switching Characteristics Updated Note 25 for better clarity. Updated Figure 10 as a single figure applicable to both CY62167G and CY62167GE. Referred Note 28, n Figure 11. Corrected typos in Note 29, 31, 36, 40.



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Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*A (Cont.)	3776318	AJU	10/30/2012	Removed "Write Cycle No. 3 (WE controlled, OE LOW)" waveform. Removed the Note "During this period the I/Os are in output state. Do not apply input signals." and its references. Removed the Note "If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state." and its references (captured in Notes 31, 36, 40) Referred Notes 38, 39, 40 in Figure 13. Updated Truth Table – CY62167G/CY62167GE (Removed references of Note 43 in BHE and BLE column). Updated Package Diagrams (spec 51-85150 (Changed revision from *G to *H)).
*В	4003550	MEMJ	05/28/2013	Updated Document Title to read as "CY62167G/CY62167GE MoBL [®] , 16-Mbit (1 M words × 16 bit / 2 M words × 8 bit) Static RAM with Error-Correcting Code (ECC)" Added 55 ns (1.8 V) device details Updated Logic Block Diagram – CY62167G. Updated Logic Block Diagram – CY62167GE. Updated Product Portfolio: Updated Product Portfolio: Updated Product Portfolio: Updated DC Electrical Characteristics: Changed typical value of I _{SB2} parameter from 5 mA to 7 mA and max value from 30 to 36. Changed typical value of I _{SB1} parameter from 3.2 μ A to 4 μ A for "V _{CC} = 1.65 to 2.2 V". Changed typical value of I _{SB2} parameter from 3.2 μ A to 4 μ A for "V _{CC} = 1.65 to 2.2 V". Updated AC Test Loads and Waveforms: Updated Data Retention Characteristics: Changed typical value of I _{CCDR} parameter from 3.2 μ A to 4 μ A for first condition only. Updated Jata Retention Characteristics: Changed typical to 29 mA from 25 mA. Updated I _{cc} Typical to 29 mA from 25 mA. Updated Figure 7. Updated Figure 7. Updated Figure 7. Updated Figure 12. Renamed "Truth Table – CY62167G" as Truth Table – CY62167G/CY62167GE and updated the same table (Added BYTE information).



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Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*C	4094068	NILE / MEMJ	10/29/2013	Updated Product Portfolio: Updated values of "Operating I _{CC} " at f = f _{MAX} (Corresponding to 55-ns spee bin only). Replaced "an error detection" with "a single-bit error detection". Updated Pin Configuration – CY62167G: Updated title of Figure 1 and Figure 2.
				Updated Pin Configuration – CY62167GE: Updated title of Figure 5. Updated DC Electrical Characteristics: Referred Note 8 in description of V _{IH} parameter. Updated Test Conditions of I _{CC} parameter (Removed f = f _{MAX} and added
				f = 22.22 MHz (45 ns) and $f = 18.18$ MHz (55 ns) and added corresponding values). Added typical and maximum values for I _{SB2} parameter for intermediate temperatures. Updated Data Retention Characteristics:
				Added Note 16 and referred the same note in I _{CCDR} parameter. Updated Ordering Information: Updated part numbers. Segregated 45 ns and 55 ns parts list in the table.
				Updated "Package Type" column (Added ERR pin location information ar Single or Dual Chip Enable information). Added Errata. Updated in new template.
*D	4274810	MEMJ	02/08/2014	Updated Operating Range: Added Note 9 and referred the same note in V _{CC} column.
*E	4292074	MEMJ / VINI	03/07/2014	Updated DC Electrical Characteristics: Changed I _{SB2} (Max) at 25C from 7uA to 4.8uA Changed I _{SB2} (typ) at 40C from 6uA to 4.5uA Changed I _{SB2} (Max) at 40C from 9uA to 8uA Added Note 10 and referred to typical values Added Note 24 and referred to write cycle timing parameters in Switching Characteristics Referred Note 31 to Figure 10. Changed title of Figure 11 from 'WE controlled' to 'WE controlled, OE LOW Added Note 32 and 33 in Figure 11. Added Note 37 in Figure 12.
				Added Note 37 in Figure 12. Added Figure 14, WE controlled write Corrected ERR table by replacing "no error in stored data" with "no single b error in stored data". Corrected ERR pin location to E3 in 'Dual Chip Enable with ERR option' in th 48-VFBGA package in Ordering Information. Added Note 41 in Figure 13 and Figure 14.
*F	4330547	AJU	04/02/2014	Changed lower limit for V_{CC} from 1.0 V to 1.2 V in I_{CCDR} conditions.



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Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*G	4397546	VINI	06/03/2014	Updated Features: Changed typical standby current from 3.2 to 4.6 μA
				Updated Product Portfolio:
				Changed I_{SB1} and I_{SB2} typical from 4.0 to 5.5 μA and maximum from 23.0 μA to 26.0 μA in the 1.8-V part
				Changed 25 °C I _{SB1} and I _{SB2} typical from 3.2 to 4.6 μ A and maximum from 4.8 μ A to 6.0 μ A in the 3.3-V and 5-V parts.
				Changed 40 °C I _{SB2} typical from 4.5 to 5.1 μ A in the 3.3-V and 5-V parts Changed 70 °C I _{SB2} typical from 9.0 to 8.4 μ A in the 3.3-V and 5-V parts. Reworded foot notes 10, 12, and 14.
				Referenced Note 12 from max values of I _{SB2} at 25 °C, 40°C and 70 °C
				Updated Data Retention Characteristics:
				Changed ICCDR typical current to 5.5 μA and maximum to 26.0 μA in the 1.8-V part
				Changed ICCDR typical current to 4.6 µA in the 3.3-V and 5-V parts.
*H	4489659	AJU	09/01/2014	Removed Errata (The Errata applicable for the Rev. ** silicon only).
				Added Errata (The Errata applicable for the Rev. *C silicon only).
*	4469360	NILE	09/18/2014	No technical updates.



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